



1. Description

1.1. Project

Project Name	rhs_acquisition
Board Name	NUCLEO-U5A5ZJ-Q
Generated with:	STM32CubeMX 6.18.0
Date	07/30/2026

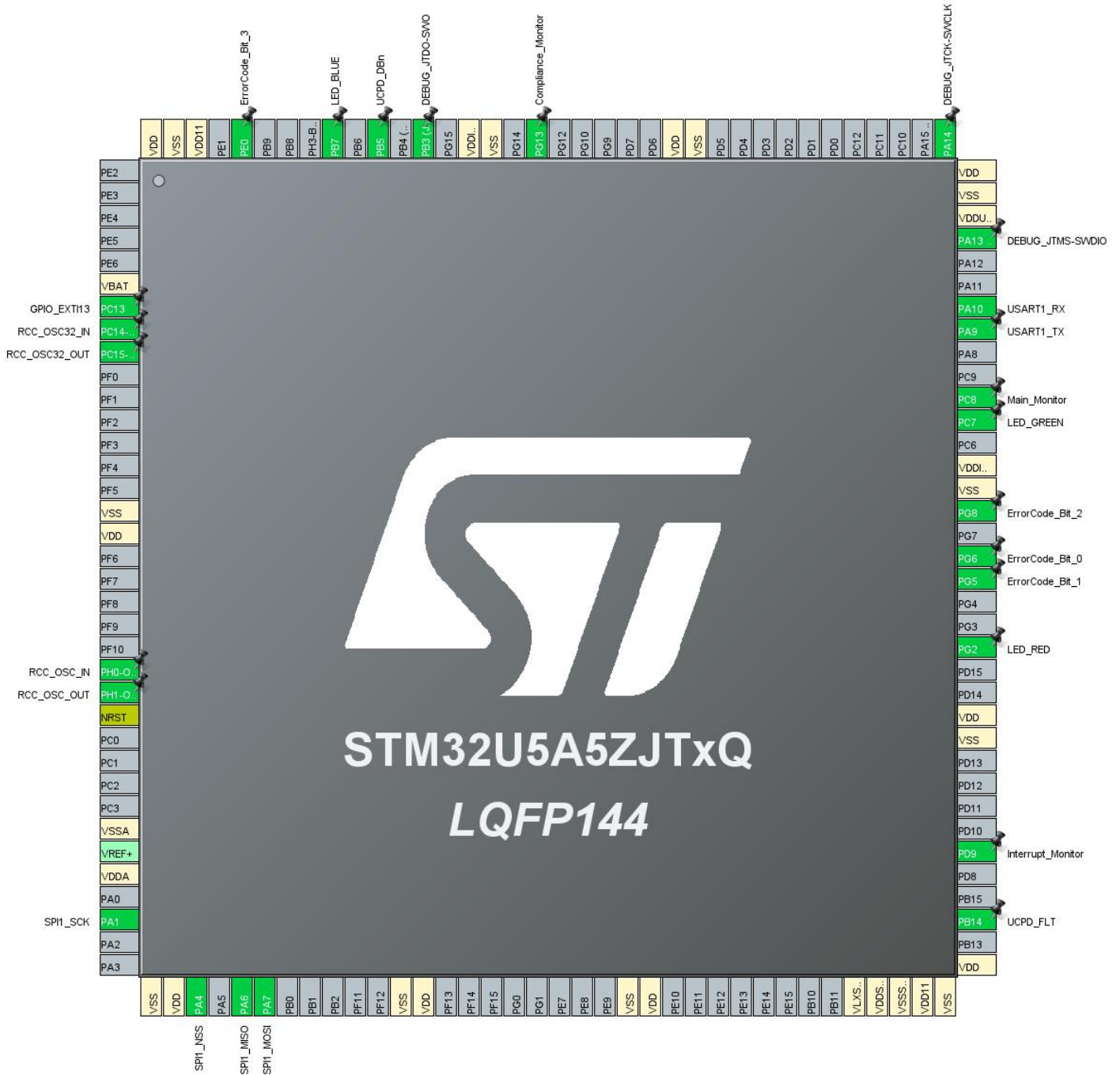
1.2. MCU

MCU Series	STM32U5
MCU Line	STM32U595/5A5
MCU name	STM32U5A5ZJTxD
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M33
---------	----------------

2. Pinout Configuration



3. Pins Configuration

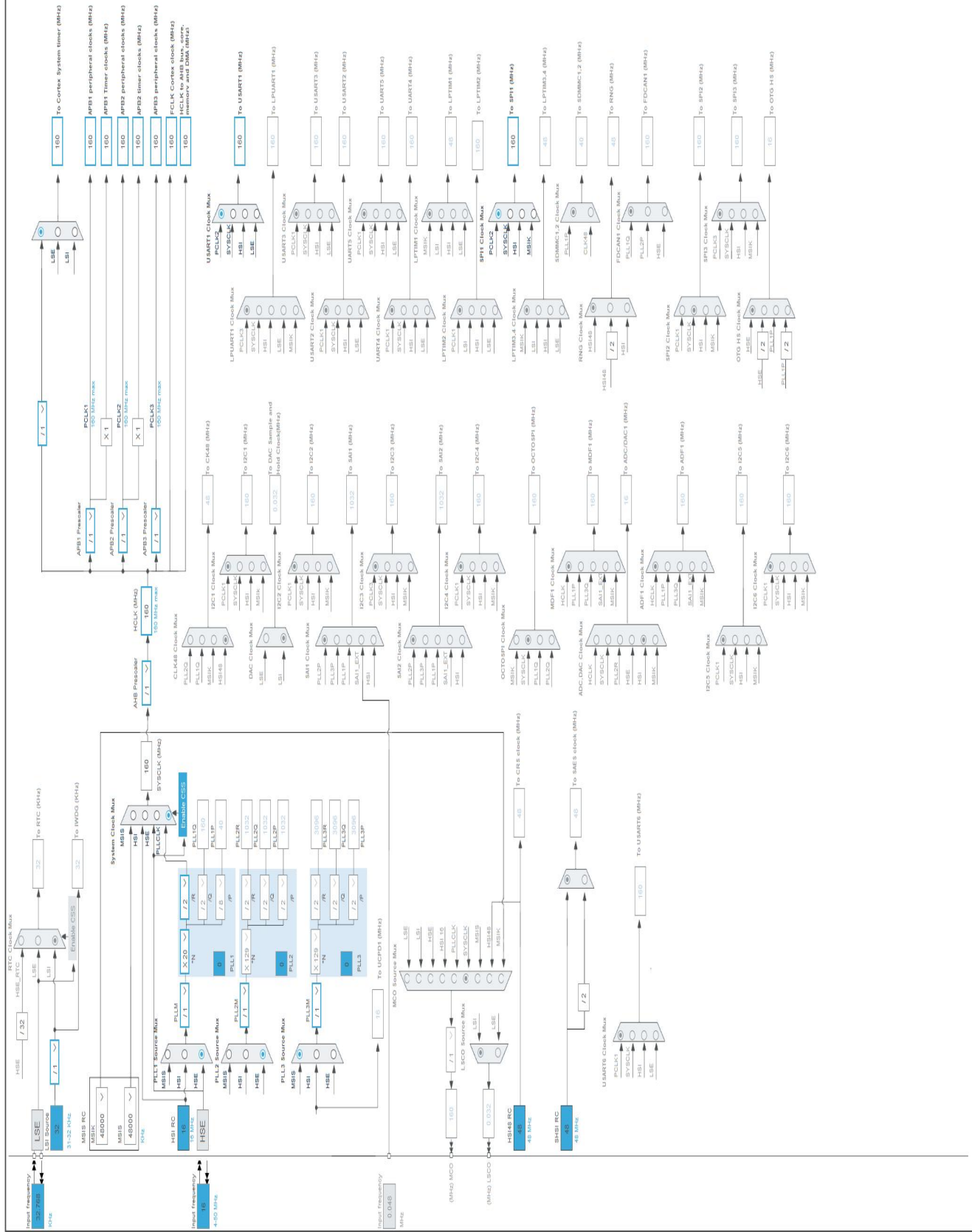
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VSSA	Power		
32	VDDA	Power		
34	PA1	I/O	SPI1_SCK	
37	VSS	Power		
38	VDD	Power		
39	PA4	I/O	SPI1_NSS	
41	PA6	I/O	SPI1_MISO	
42	PA7	I/O	SPI1_MOSI	
48	VSS	Power		
49	VDD	Power		
58	VSS	Power		
59	VDD	Power		
68	VLXSMPS	Power		
69	VDDSMPS	Power		
70	VSSSMPS	Power		
71	VDD11	Power		
72	VSS	Power		
73	VDD	Power		
75	PB14 *	I/O	GPIO_Input	UCPD_FLT
78	PD9 *	I/O	GPIO_Output	Interrupt_Monitor
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Output	LED_RED
90	PG5 *	I/O	GPIO_Output	ErrorCode_Bit_1
91	PG6 *	I/O	GPIO_Output	ErrorCode_Bit_0
93	PG8 *	I/O	GPIO_Output	ErrorCode_Bit_2
94	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
95	VDDIO2	Power		
97	PC7 *	I/O	GPIO_Output	LED_GREEN
98	PC8 *	I/O	GPIO_Output	Main_Monitor
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
105	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
120	VSS	Power		
121	VDD	Power		
127	PG13 *	I/O	GPIO_Output	Compliance_Monitor
129	VSS	Power		
130	VDDIO2	Power		
132	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
134	PB5 *	I/O	GPIO_Output	UCPD_DBn
136	PB7 *	I/O	GPIO_Output	LED_BLUE
140	PE0 *	I/O	GPIO_Output	ErrorCode_Bit_3
142	VDD11	Power		
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration

RIF configuration not available for STM32U5A5ZJTxxQ



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32U5
Line	STM32U595/5A5
MCU	STM32U5A5ZJTxD
Datasheet	not yet available

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

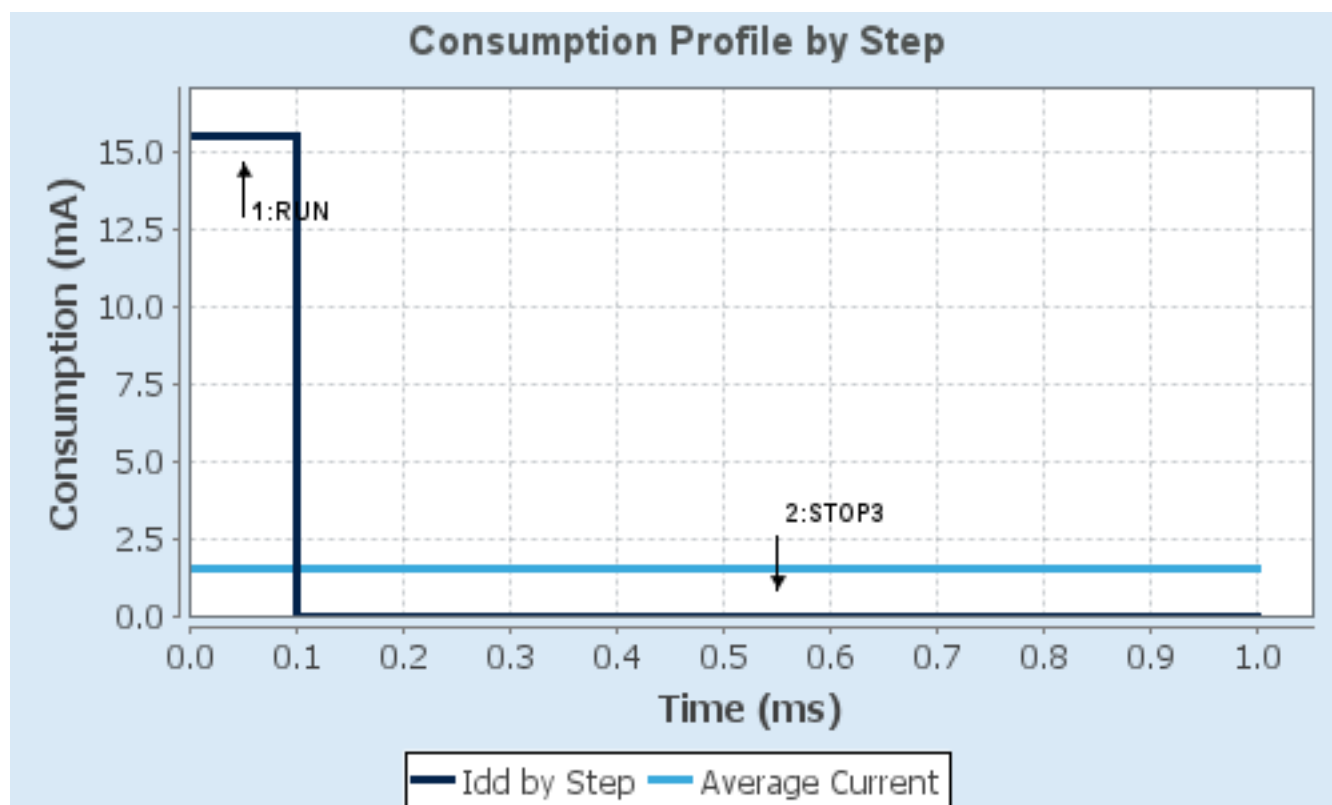
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP3
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Medium	NoRange/SMPS
Fetch Type	FLASH- PwrDwnBank2/ART/Cache- 2Ways/AlgoType- ReducedCode	FLASH
CPU Frequency	160 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_RAM_RETENTION	ALL_CLOCKS_OFF
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	15.5 mA	1.85 μ A
Duration	0.1 ms	0.9 ms
DMIPS	240.0	0.0
Ta Max	138.42	140
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.55 mA
Battery Life	2 months, 30 days, 5 hours	Average DMIPS	24.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	rhs_acquisition
Project Folder	C:\Users\lfoyl\Desktop\Software_Projects\STM32_Projects\U5_workspace\rhs_a
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_U5 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_GPDMA1_Init	GPDMA1
4	MX_ICACHE_Init	ICACHE
5	MX_TIM3_Init	TIM3
6	MX_USART1_UART_Init	USART1
7	MX_SPI1_Init	SPI1

3. Peripherals and Middlewares Configuration

3.1. DEBUG

Debug: Trace Asynchronous Sw

3.2. ICACHE

Mode: 1-way (direct mapped cache)

3.3. LPBAM

mode: LPBAM Scenario uses resources from Smart Run Domain only

mode: LPBAM Scenario is hosted by LPDMA1

3.4. LPBAMQUEUE

mode: QUEUE MODE

3.4.1. Parameter Settings:

DMA Channel Configuration:

Priority	Low
----------	-----

DMA Channel Interrupt Configuration:

Data Transfer Error Interrupt	Disable
Update Link Error Interrupt	Disable
User Setting Error Interrupt	Disable
Transfer Complete Interrupt	Disable
Trigger Overrun Interrupt	Disable

3.5. MEMORYMAP

mode: Activated

3.6. PWR

mode: Dead Battery Signals disabled

mode: Power saving mode

mode: Privilege attributes

3.6.1. Power Saving:

System power supply:

Power Regulator	SMPS *
-----------------	--------

SRAM power down in Run mode:

SRAM1 power down in Run mode	Disable
SRAM2 power down in Run mode	Disable
SRAM3 power down in Run mode	Disable
SRAM4 power down in Run mode	Disable
SRAM5 power down in Run mode	Disable

SRAM power down in Stop mode:

SRAM1 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page8 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page9 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page10 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page11 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page12 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM2 Page1 power down in Stop (0, 1, 2) mode	Disable
SRAM2 Page2 power down in Stop (0, 1, 2) mode	Disable
SRAM3 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page8 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page9 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page10 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page11 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page12 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page13 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page8 power down in Stop (0, 1, 2, 3) mode	Disable

SRAM5 Page9 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page10 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page11 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page12 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM5 Page13 power down in Stop (0, 1, 2, 3) mode	Disable
ICACHE power down in Stop (0, 1, 2, 3) mode	Disable
DCACHE1 power down in Stop (0, 1, 2, 3) mode	Disable
DCACHE2 power down in Stop (0, 1, 2, 3) mode	Disable
DMA2D RAM power down in Stop (0, 1, 2, 3) mode	Disable
PKA32 RAM power down in Stop (0, 1, 2, 3) mode	Disable
PERIPH RAM power down in Stop (0, 1, 2, 3) mode	Disable
GRAPHIC PRAM power down in Stop (0, 1, 2, 3) mode	Disable
DSI RAM power down in Stop (0, 1, 2, 3) mode	Disable
SRAM fast wakeup:	
SRAM4 fast wakeup from Stop (0, 1, 2, 3) modes	Disable

3.6.2. PWR Privilege :

Privilege PWR:

Privilege of PWR Secure Items	Disable
Privilege of PWR Non-Secure Items	Disable
PWR Privilege	Disable

3.6.3. PWR Security:

Secure PWR:

Wake-Up 1 secure protection	Disable
Wake-Up 2 secure protection	Disable
Wake-Up 3 secure protection	Disable
Wake-Up 4 secure protection	Disable
Wake-Up 5 secure protection	Disable
Wake-Up 6 secure protection	Disable
Wake-Up 7 secure protection	Disable
Wake-Up 8 secure protection	Disable
Voltage detection and monitoring secure protection	Disable
Pull-up/pull-down secure protection	Disable
Low power modes secure protection	Disable
Backup domain secure protection	Disable

3.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.7.1. RCC Privilege :

Privilege RCC:

Privilege of RCC Non-Secure Items	Disable
-----------------------------------	---------

3.7.2. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	16
MSIS/MSIK Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
-------------------------------	---------------------------------

PLL1/2/3 Parameters:

PLL1M BOOST EPOD Clock Divider	1
PLL1 input frequency range	Between 8 and 16 MHz

Low Power Parameters:

MSI in Stop mode	Disabled
HSI in Stop mode	Disabled

3.8. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

3.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	32 Bits *

First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	8 *
Baud Rate	20.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Autonomous Mode:	
State	Disable
CRC Parameters:	
CRC Calculation	Disabled
Advanced Parameters:	
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	04 Cycle *
Master Receiver Auto Susp	Enable *
Master Keep Io State	Master Keep Io State Enable *
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

3.9. SYS

Timebase Source: SysTick

3.10. TIM3

Channel1: Output Compare No Output

3.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value)	8000 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
--------------------	---------

Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	0
Output compare preload	Disable
CH Polarity	High

3.11. USART1

Mode: Asynchronous

3.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	10000000 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Transmit Only *
Over Sampling	8 Samples *
Single Sample	Enable *
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Autonomous Mode	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Disable *
DMA on RX Error	Disable *
MSB First	Disable

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA1	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UCPD_FLT
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Interrupt_Monitor
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ErrorCode_Bit_1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ErrorCode_Bit_0
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ErrorCode_Bit_2
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	Main_Monitor
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Compliance_Monitor
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UCPD_DBN
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_BLUE
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ErrorCode_Bit_3

4.2. GPDMA1

Channel 13 - 8 Words Internal FIFO / 2D addressing: Standard Request Mode

Channel 12 - 8 Words Internal FIFO / 2D addressing: Standard Request Mode

Channel 0 - 2 Words Internal FIFO : Standard Request Mode

4.2.1. All Channels:

Channel 0:

Request GPDMA1_REQUEST_USART1_TX

Channel 12:

Request GPDMA1_REQUEST_SPI1_TX

Channel 13:

Request GPDMA1_REQUEST_SPI1_RX

4.2.2. SECURITY:

CH13:

Enable Channel as Privileged NON PRIVILEGED

CH12:

Enable Channel as Privileged NON PRIVILEGED

CH0:

Enable Channel as Privileged NON PRIVILEGED

4.2.3. CH13:

Circular configuration:

Circular Mode Disable

Request Configuration:

Request	SPI1_RX *
DMA Handle in IP Structure	hdmarx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	Low
Transaction Mode	Normal
Direction	Peripheral To Memory

Source Data Setting:

Source Address Increment After Transfer	Disabled
Data Width	Word *
Burst Length	1
Allocated Port for Transfer	Port 0

Destination Data Setting:

Destination Address Increment After Transfer	Enabled *
Data Width	Word *
Burst Length	1
Allocated Port for Transfer	Port 0

Data Handling:

Data Handling Configuration	Disable
-----------------------------	---------

Trigger:

Trigger Configuration	Disable
-----------------------	---------

2D Addressing:

Configuration	Disabled
---------------	----------

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block
---------------------------	---

4.2.4. CH12:

Circular configuration:

Circular Mode	Disable
---------------	---------

Request Configuration:

Request	SPI1_TX *
DMA Handle in IP Structure	hdmatx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	Low
Transaction Mode	Normal
Direction	Memory To Peripheral *

Source Data Setting:

Source Address Increment After Transfer	Enabled *
Data Width	Word *
Burst Length	1
Allocated Port for Transfer	Port 0

Destination Data Setting:

Destination Address Increment After Transfer	Disabled
Data Width	Word *
Burst Length	1
Allocated Port for Transfer	Port 0

Data Handling:

Data Handling Configuration	Disable
-----------------------------	---------

Trigger:

Trigger Configuration	Disable
-----------------------	---------

2D Addressing:

Configuration	Disabled
---------------	----------

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block
---------------------------	---

4.2.5. CH0:

Circular configuration:

Circular Mode	Disable
---------------	---------

Request Configuration:

Request	USART1_TX *
DMA Handle in IP Structure	hdmatx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	Very High *
Transaction Mode	Normal
Direction	Memory To Peripheral *

Source Data Setting:

Source Address Increment After Transfer	Enabled *
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	Port 0

Destination Data Setting:

Destination Address Increment After Transfer	Disabled
Data Width	Byte

Burst Length	1
Allocated Port for Transfer	Port 0
Data Handling:	
Data Handling Configuration	Disable
Trigger:	
Trigger Configuration	Disable
Transfer Event Configuration:	
Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

4.3. LINKEDLIST

4.4. LPDMA1

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI Line13 interrupt	true	0	0
GPDMA1 Channel 0 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
USART1 global interrupt	true	0	0
GPDMA1 Channel 12 global interrupt	true	0	0
GPDMA1 Channel 13 global interrupt	true	0	0
Flash non-secure global interrupt	unused		
RCC non-secure global interrupt	unused		
FPU global interrupt	unused		
Instruction cache global interrupt	unused		

4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI Line13 interrupt	false	true	true
GPDMA1 Channel 0 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
SPI1 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
USART1 global interrupt	false	true	true
GPDMA1 Channel 12 global interrupt	false	true	true
GPDMA1 Channel 13 global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32u5_bsd.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32u5-ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32u5_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32u5-series-product-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32u5-mcu-lines-for-advanced-graphics.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32ulp.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32u5.pdf
Security Advisory	https://www.st.com/resource/en/security_advisory/sa0055-sfi-security-enhancement-for-stm32h523533-microcontrollers-stm32u5-series-and-stm32l5-series-stmicroelectronics.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1474-security-bulletin-tn1474stpsirt-information-on-softwarebased--microarchitectural-timing-sidechannel-attacks-on-mcus-with-trustzone-for--armv8m-stmicroelectronics.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-

tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf

Security Bulletin https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5447-overview-of-secure-boot-and-secure-firmware-update-solution-on-arm-trustzone-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5645-stm32u5-series-power-optimization-using-lpbam-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5834-lc-sensor-metering-implementation-on-stm32u5-series-featuring-lpbam-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4991-how-to-wake-

up-an-stm32-microcontroller-from-lowpower-mode-with-the-usart-or-the-lpuart-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5766-migrating-within-stm32u5-series-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4838-introduction-to-memory-protection-unit-management-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5325-how-to-use-the-cordic-to-perform-mathematical-functions-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5371-migration-from-stm32l5-series-to-stm32u5-series-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4879-introduction-to-usb-hardware-and-pcb-guidelines-using-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5373-getting-started-with-stm32u5-mcu-hardware-development-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5372-migrating-from-stm32l4-and-stm32l4--to-stm32u5-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5342--how-to-use-error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5652-how-to-optimize-power-consumption-on-stm32u5-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5701-introduction-to-stm32cube-mcu-package-examples-for-stm32u5-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4894-how-to-use-eeeprom-emulation-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5537-how-to-use-adc-

oversampling-techniques-to-improve-signal-to-noise-ratio-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5632-migrating--a-graphic-application-from-stm32l4-to-stm32u59x5ax5fx5gx-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4992-introduction-to-secure-firmware-install-sfi-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5405-how-to-use-fdcan-bootloader-protocol-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5690-how-to-use-vrefbuf-peripheral-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4230-introduction-to-random-number-generation-validation-using-the-nist-statistical-test-suite-for-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcus-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3236-how-to-increase-the-number-of-touchkeys-for-touch-sensing-applications-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3960-guidelines-for-esd-for-touch-sensing-applications-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4013-introduction-to-timers-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4277-how-to-use-pwm-shutdown-for-motor-control-and-digital-power-conversion-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4299-how-to-improve-conducted-noise-robustness-for-touch-sensing-applications-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4310-how-to-choose-the-sampling-capacitor-for-touch-sensing-applications-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4312-how-to-design-surface-sensors-for-touch-sensing-applications-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4316-how-to-tune-touch-sensing-applications-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4635-how-to-optimize-lpuart-power-consumption-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4861-introduction-to-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4908-getting-started-with-usart-automatic-baud-rater-detection-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4943-how-to-use-chromart-accelerator-to-refresh-an-lcdtft-display-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5156-introduction-to-security-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5593-how-to-use-the-gpdma-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5816-how-to-build-a-lpbam-application-on-stm32u5-mcus-using-stm32cubemx-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5543-guidelines-for-enhanced-spi-communication-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5348-introduction-to-fdcan-peripherals-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/cd00211314-how-to-optimize-the-adc-accuracy-in-the-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack2-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5020-introduction-to-digital-camera-interface-dcml-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4566-how-to-extend-the-dac-performance-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5105-getting-started-with-touch-sensing-control-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5347-introduction-to-arm-trustzone-features-on-stm32l5-stm32u5-and-stm32u3-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5676-how-to-calibrate-internal-rc-oscillators-on-stm32u3-and-stm32u5-series-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an6012-migrating-between-stm32u5-and-stm32u3-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5421-getting-started-with-stm32-mcus-and-armtrustzone-development-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5647-the-goertzel-algorithm-to-compute-individual-terms-of-the-discrete-fourier-transform-dft-in-stm32-products-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2606-introduction-to-system-memory-boot-mode-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5036-guidelines-for-thermal-management-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3126-how-to-use-dac-for-audio-and-waveform-generation-on-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3155-how-to-use-uart-protocol-in-bootloader-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3156-how-to-use-usb-ldf-protocol-in-bootloader-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4286-how-to-use-spi-protocol-in-bootloader-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4759-introduction-to

using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4776-how-to-use-generalpurpose-timer-peripheral-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4989-introduction-to-debug-toolbox-for-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5050-getting-started-with-octospi-hexadecapi-and-xspi-interfaces-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5212-how-to-use-the-cache-to-optimize-performance-and-power-efficiency-on-stm32-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5795-how-to-use-multifunction-digital-filter-mdf-to-capture-sound-on-stm32-mcus-stmicroelectronics.pdf

Errata Sheets https://www.st.com/resource/en/errata_sheet/es0553-stm32u59xxx-and-stm32u5axxx-device-errata-stmicroelectronics.pdf

Datasheet <https://www.st.com/resource/en/datasheet/dm00745736.pdf>

Programming Manuals https://www.st.com/resource/en/programming_manual/pm0264-stm32-cortexm33-mcus-and-mpus-programming-manual-stmicroelectronics.pdf

Reference Manuals https://www.st.com/resource/en/reference_manual/rm0456-stm32u5-series-armbased-32bit-mcus-stmicroelectronics.pdf

Technical Notes & Articles https://www.st.com/resource/en/technical_note/tn1163-description-of-wlcsp-for-microcontrollers-and-recommendations-for-its-use-stmicroelectronics.pdf

Technical Notes & Articles https://www.st.com/resource/en/technical_note/tn1205-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-fpn-packages-stmicroelectronics.pdf

Technical Notes & Articles https://www.st.com/resource/en/technical_note/tn1206-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-qfp-packages-stmicroelectronics.pdf

Technical Notes & Articles https://www.st.com/resource/en/technical_note/tn1207-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-so-packages-stmicroelectronics.pdf

	stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1208-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-tssop-and-ssop-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1433-reference-device-marking-schematics-for-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1204-tape-and-reel-shipping-media-for-stm32-devices-in-bga-packages-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um2875-stm32u5-series-safety-manual-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um3387-stm32u5xstm32wba5x-security-guidance-for-sesip-level-3-certification-stmicroelectronics.pdf