intan TECHNOLOGIES, LLC

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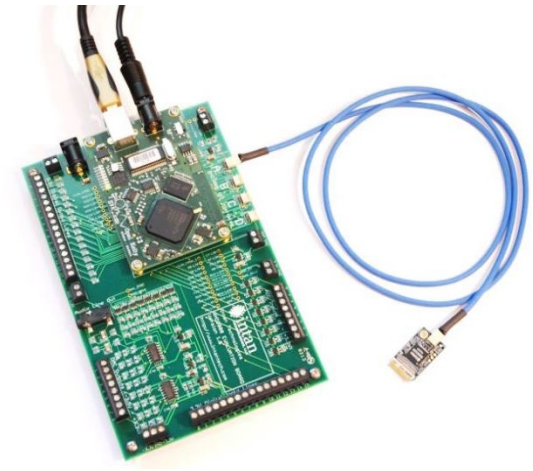
RHD2000-EVAL



Application Note: I/O Voltage Level Shifting

15 April 2013; updated 27 May 2021

Q:

The RHD USB interface board includes general-purpose digital I/O, but these lines operate with 3.3V logic levels. How can these signals be scaled to and from 5.0V logic levels?

The interface board also includes analog-to-digital converters, but the range of these ADCs is restricted to positive voltages in the range of 0 – 3.3V. Is there a circuit that can adapt these ADCs to sense voltages in the range of ±3.3V or ±5.0V?

A:

This application note presents relatively simple circuits that can be used to interface the 3.3V signals on the RHD USB interface board to a wider range of voltage levels. All the circuits shown in this document can be built using breadboard, wire-wrap, or hand soldering techniques. None of these circuits operate at high speeds (the maximum sampling rate of the RHD USB interface board is 30 kS/s), so users need not worry about parasitic capacitances, ground planes, or other high-performance circuit building techniques. We have purposely selected parts that are available in DIP packages so that surface-mount assembly can be avoided to ease assembly.

Converting 3.3V Digital Output Signals to 5.0V

The RHD USB interface board allocates 16 output lines from the Spartan-6 FPGA as general-purpose digital outputs. These signals are controlled using the **setTtlOut** function in the Rhythm C++ API (see the **Rhythm API** document for more information). Since the FPGA operates with 3.3V I/O, these signals operate between ground and 3.3V.

A circuit for scaling these 3.3V signals to 5.0V signals is shown in Figure 1 on the following page. The circuit uses an MC14504B level shifter integrated circuit (IC) that contains six digital voltage translator circuits. The input pins (**Ain** – **Fin**) receive digital signals operating on a voltage scale defined by the **VCC** power pin. These signals are shifted to the voltage scale defined by the **VDD** power pin and appear on the output pins (**Aout** – **Fout**). It is recommended that 0.1 µF capacitors to ground be placed close to the power pins to supply rapid currents when switching occurs.

The 50 Ω resistors are optional, but will reduce signal reflections if the output pins are connected to a long coaxial cable. If long twisted pairs or ribbon cables are used, a resistor value of 100 Ω or 200 Ω may work better to dampen reflections.

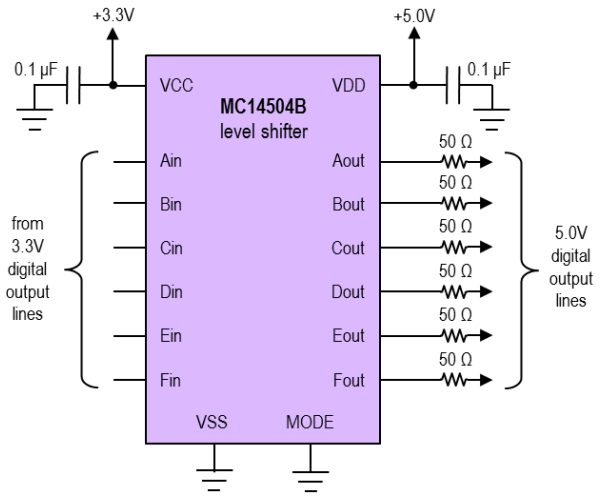


Figure 1. Digital level shifter circuit to convert 3.3V logic signals to 5.0V logic signals.

The MC14504B chip is widely available in both 16-pin DIP and SOIC (surface mount) packages. Digi-Key part numbers are MC14504BCPGOS-ND (for the DIP package) and MC14504BDR2GOSCT-ND (for the SOIC package). More information on this part can be found by searching for the MC14504B datasheet. The MC14504B chip introduces a delay of approximately 200 ns to digital signals in this configuration; faster level-shifter chips are available from many companies. If the MC14504B is not available, the Texas Instruments CD4504B (Digi-Key part number 296-3527-5-ND for the DIP version) may be used in its place.

An alternate level-shifting IC containing eight level shifters in one 24-pin package is the SN74LVC4245A, but this part is only available in surface-mount packages.

Digital Input Signals

The RHD USB interface board also includes 16 general-purpose digital input lines. These inputs are sampled in synchrony with all amplifier channels when using the RHD2000 interface software, and they may also be accessed using the **getTtlIn** function in the Rhythm C++ API. The FPGA operates with 3.3V I/O, but it can tolerate 5V logic signals. Standard 5V TTL digital signals may be connected to the digital inputs.

Converting ±3.3V Analog Input Signals to 0 – 3.3V Signals

The RHD USB interface board includes eight analog input lines that use analog-to-digital converters (ADCs) to sample voltages in the range of 0 – 3.3V. These voltages are sampled in synchrony with the amplifier channels when using Intan data acquisition software, and are also accessible using the Rhythm C++ API.

In many practical applications, both negative and positive voltages may need to be observed (e.g., an AC-coupled sensor with a zero-volt baseline signal). A circuit that scales voltage in the range of ±3.3V to the 0 – 3.3V range required by the interface board ADCs is shown in Figure 3 on the following page.

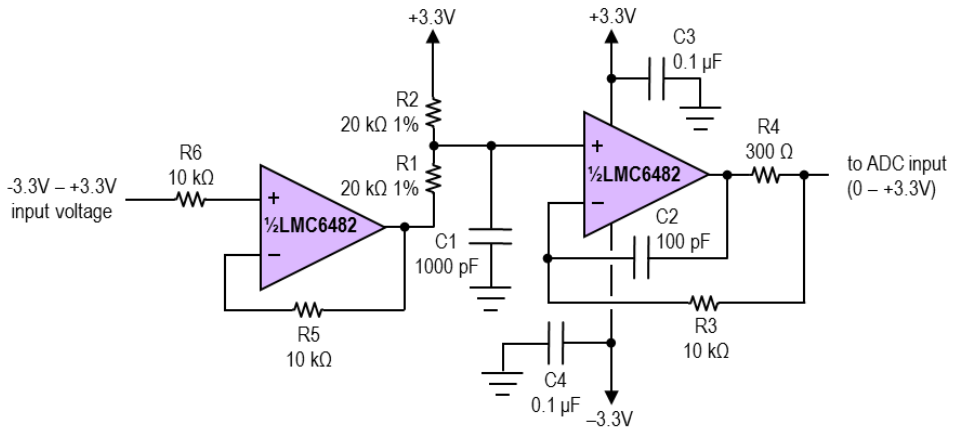


Figure 3. Circuit to scale analog voltages in the range of ±3.3V to the range of 0 – 3.3V for sensing by the RHD USB interface board. The label "1%" indicates that resistors with 1% (or better) precision should be used for particular resistors.

This circuit uses the LMC6482 operational amplifier IC which contains two independent op amps. Importantly, these op amps operate "rail to rail" over the entire ±3.3V power supply range. They also have very small input bias currents and small voltage offsets. The LMC6482 is available in both DIP and SOIC (surface mount) packages. The Digi-Key part number for the 8-pin DIP package is LMC6482AIN/NOPB-ND; the part number for the 8-pin SOIC is LMC6482IMX/NOPBCT-ND.

The op amp on the left of Figure 3 is a unity-gain buffer that drives R1 and R2; these resistors scale the voltage by half and shift its range to 0 – 3.3V. The capacitor C1, in combination with the parallel combination of R1 and R2 (i.e., 10 kΩ), set a low-pass filter frequency close to 15 kHz, which is appropriate for anti-alias filtering at a sample rate of 30 kS/s. The value of C1 may be increased to lower this filter frequency for lower sample rates.

The op amp on the right of Figure 3, along with R3, R4, and C2, form a unity-gain buffer capable of rapidly driving the capacitive input of an ADC. Capacitors C3 and C4 filter the ±3.3V power supply (which may be obtained from the RHD USB interface board) and should be placed in close proximity to the LMC6482 chip. For best accuracy, the +3.3V supply should be taken from the connector next to the analog inputs on the RHD USB interface board, since it is this supply that powers the ADCs. (The -3.3V supply can be taken from the connector between the digital inputs and analog outputs.)

Resistor R6 is used to protect the input op amp against over-voltage conditions, and R5 is used to ensure that the two inputs to the op amp see the same resistance to minimize voltage offsets. The input resistance of this circuit is greater than 10^{12} Ω owing to the CMOS inputs of the LMC6482 op amps. (See the LMC6482 datasheet for more information on this device.)

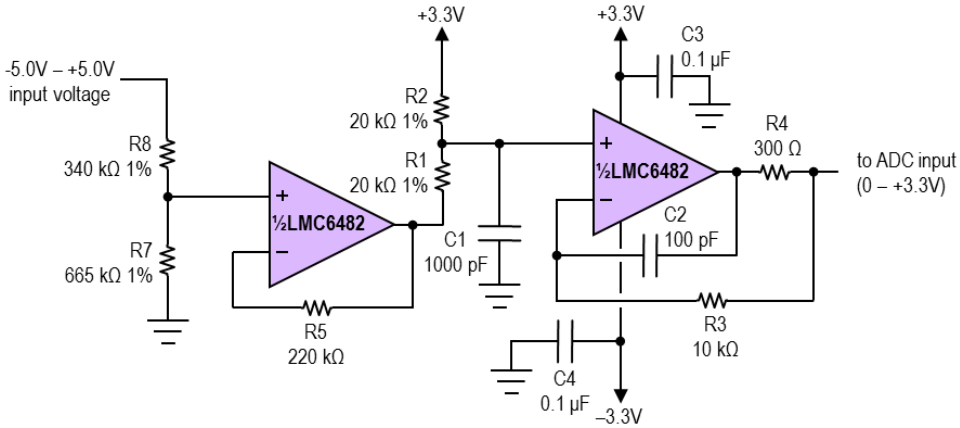


Figure 4. Circuit to scale analog voltages in the range of ±5.0V to the range of 0 – 3.3V for sensing by the RHD USB interface board. The circuit is similar to the one in Figure 3, but the value of R5 has changed, R6 has been removed, and R7 and R8 have been added.

Converting ±5.0V Analog Input Signals to 0 – 3.3V Signals

In some applications, a wider range of analog voltages must be observed. The circuit shown in Figure 4 on the previous page scales voltages in the range of ±5.0V to the 0 – 3.3V range of the RHD USB interface board ADCs.

This circuit is very similar to the one shown in Figure 3. A voltage divider consisting of resistor R7 and R8 have been added, R6 has been removed (though it could be kept), and the value of R5 has been changed to match the resistance seen by the positive input of the op amp (i.e., the parallel combination of R7 and R8).

The resistor divider formed by R7 and R8 scales the voltage down by a factor of 0.66, which maps ±5.0V to ±3.3V. The rest of the circuit works identically to the circuit from Figure 3. This circuit has a lower input resistance than the previous circuit: approximately 1.0 MΩ. If an extremely high input resistance is needed, then another unity-gain op amp must be added to the input as a buffer, but this op amp would have to be powered from a ±5.0V power supply to follow signals over this range. The LMC6482 can be operated from a ±5.0V supply, but the RHD USB interface board provides only a +5.0V voltage supply and not a -5.0V supply.

Alternate values of R7 and R8 may be selected to scale a wider range of voltages to the 0 – 3.3V ADC level. For example, using R7 = 330 kΩ and R8 = 665 kΩ (both standard 1% precision resistance values) allows voltages over the range of ±10V to be accepted.