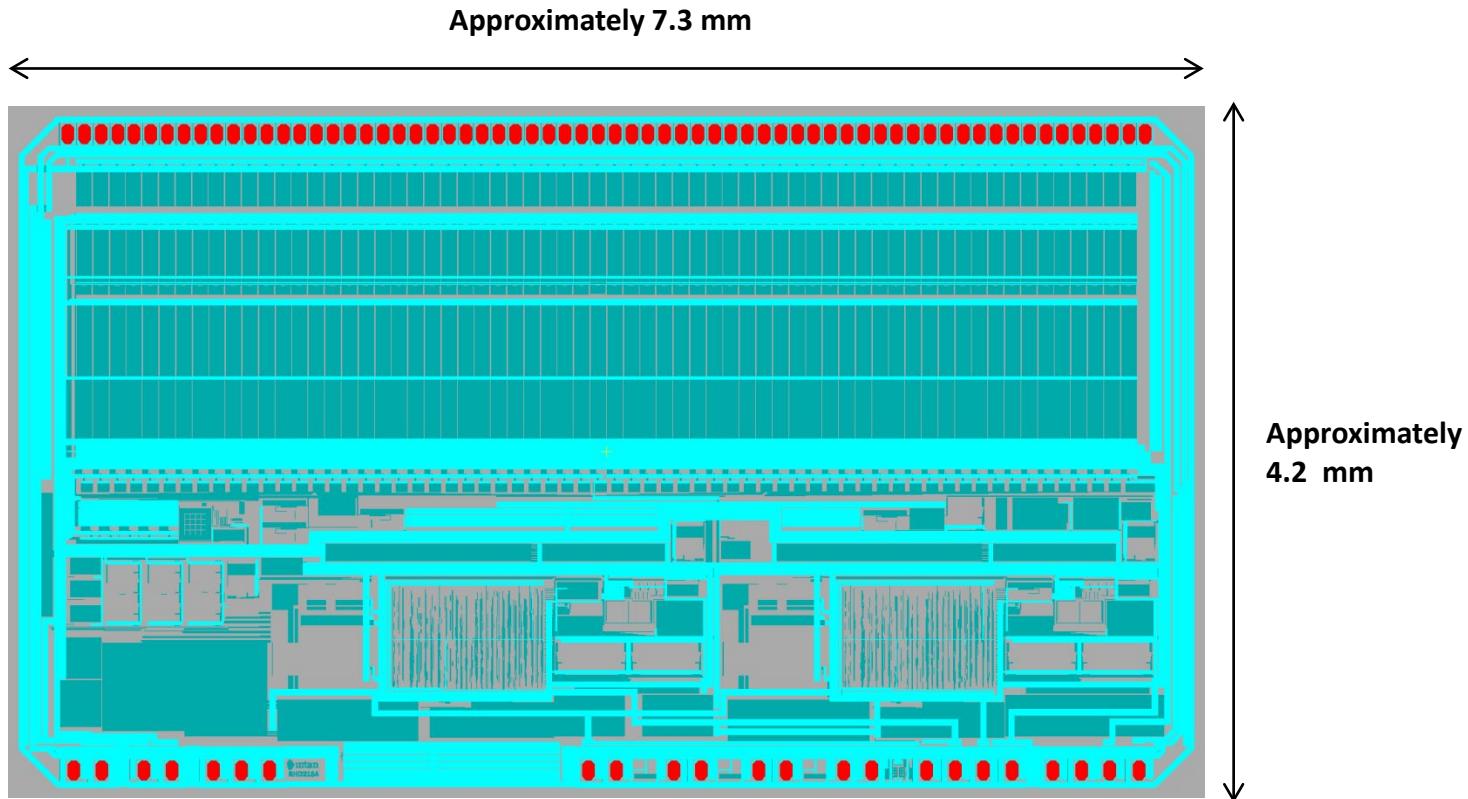


# Intan Technologies RHD2164 Bare Die



**Gray** = approximate outline of die (may vary from die to die due to variations in sawing)

**Yellow Cross** = center of design (may not coincide precisely with center of die due to variations in sawing)

**Blue, Green** = top metal layers (highly visible)

**Red** = glass openings for bond pads

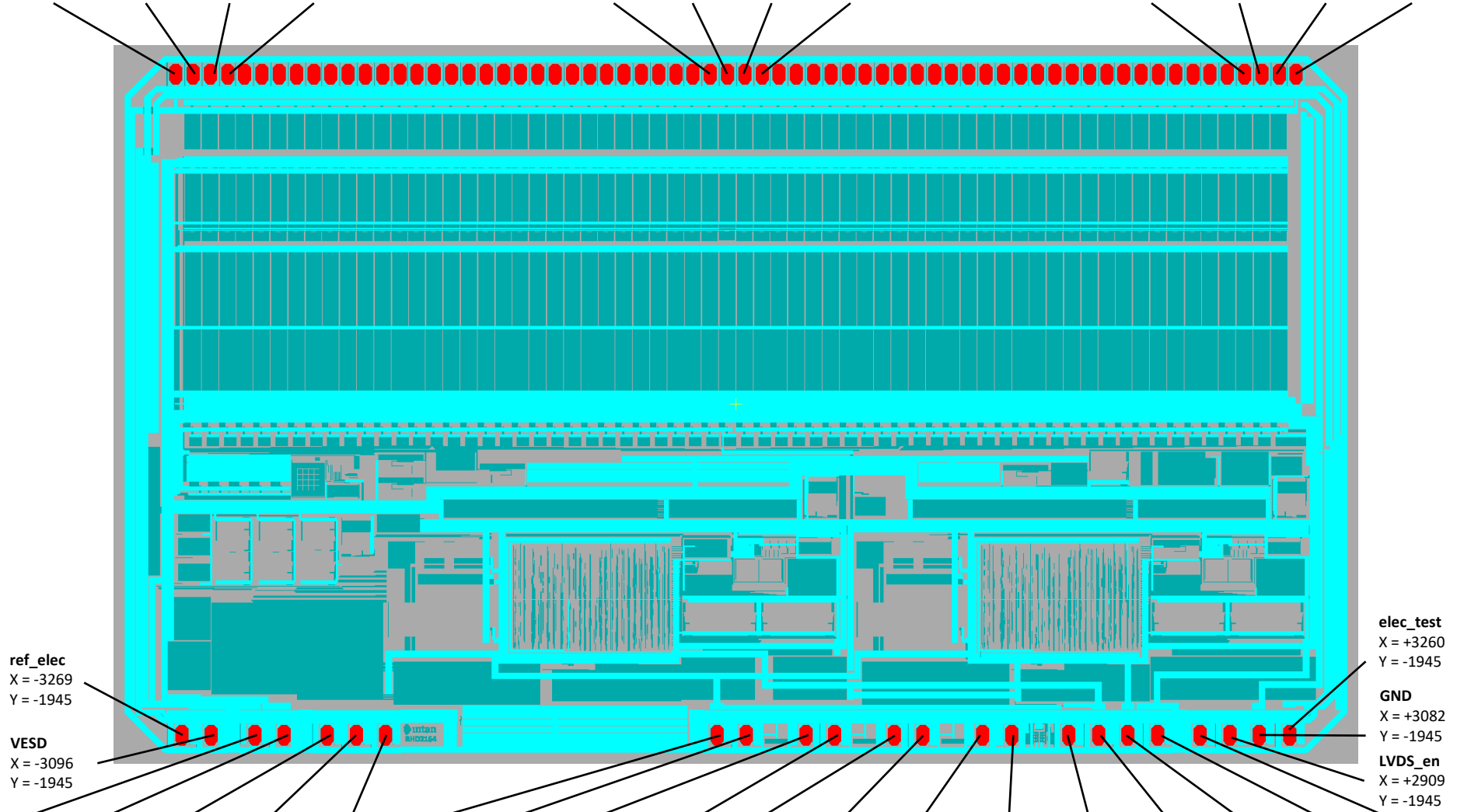
Each die is 0.20 mm (8 mils) thick

# RHD2164

# Coordinates of Bond Pad Centers, Relative to Center of Design

dimensions in microns

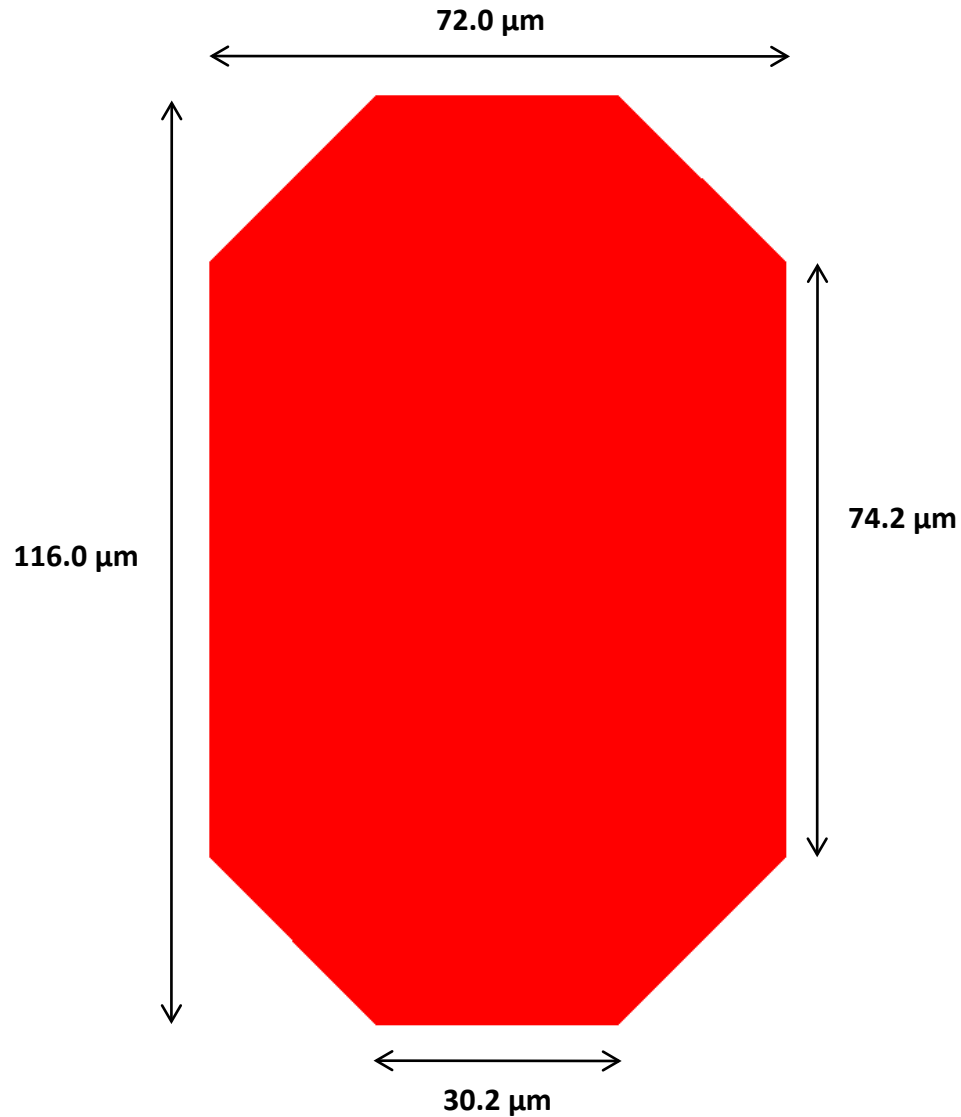
<b>ref_elec</b> X = -3302.0 Y = +1945	<b>in0</b> X = -3200.4 Y = +1945	<b>in1</b> X = -3098.8 Y = +1945	<b>in2</b> X = -2997.2 Y = +1945	amplifier pad pitch is 101.6 microns (4.000 mil) ● ● ● ● ● ●				<b>in30</b> X = -152.4 Y = +1945	<b>in31</b> X = -50.8 Y = +1945	<b>in32</b> X = +50.8 Y = +1945	<b>in33</b> X = +152.4 Y = +1945	amplifier pad pitch is 101.6 microns (4.000 mil) ● ● ● ● ● ●				<b>in61</b> X = +2997.2 Y = +1945	<b>in62</b> X = +3098.8 Y = +1945	<b>in63</b> X = +3200.4 Y = +1945	<b>ref_elec</b> X = +3302.0 Y = +1945
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<b>ref_elec</b> X = -3269 Y = -1945	<b>VESD</b> X = -3096 Y = -1945	<b>GND</b> X = -2837 Y = -1945	<b>VDD</b> X = -2664 Y = -1945	<b>auxin1</b> X = -2411 Y = -1945	<b>auxin2</b> X = -2238 Y = -1945	<b>auxin3</b> X = -2065 Y = -1945	<b>GND</b> X = -112 Y = -1945	<b>CS-</b> X = +61 Y = -1945	<b>CS+</b> X = +415 Y = -1945	<b>SCLK-</b> X = +580 Y = -1945	<b>SCLK+</b> X = +934 Y = -1945	<b>MOSI-</b> X = +1099 Y = -1945	<b>MOSI+</b> X = +1453 Y = -1945	<b>MISO-</b> X = +1626 Y = -1945	<b>MISO+</b> X = +1964 Y = -1945	<b>VDD</b> X = +2137 Y = -1945	<b>VDD</b> X = +2310 Y = -1945	<b>ADC_ref</b> X = +2483 Y = -1945	<b>auxout</b> X = +2736 Y = -1945	<b>elec_test</b> X = +3260 Y = -1945	<b>GND</b> X = +3082 Y = -1945	<b>LVDS_en</b> X = +2909 Y = -1945
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## Bond Pad Dimensions

Bond pad metal: AlCu (99.5% aluminum, 0.5% copper) Thickness: 2.9  $\mu\text{m}$



Minimum bond pad pitch (center to center) on RHD2164: 101.6  $\mu\text{m}$  (4.000 mil)

Each RHD2164 die has three bondpads for the reference electrode connection (labeled **ref\_elec**). These are located in the upper left, upper right, and lower left corners of the chip. These pads are connected internally on the chip, so only **one** of these pads needs to be bonded. There is no advantage to bonding more than one of these pads. Multiple bond pads are provided only for circuit board layout convenience.

There are three ground pads and three power pads (labeled **GND** and **VDD**). **All six** of these pads **must** be bonded and connected to the appropriate supply voltages for proper operation. An off-chip 100 nF capacitor between ground and VDD should be placed less than 1 cm from the lower edge of the chip. For best operation, this capacitor should have an X5R or X7R dielectric and should be rated for at least 16V. If non-LVDS (standard CMOS) signaling is used, it is recommended that two 100 nF capacitors be used: one near the lower left corner of the chip and one near the lower right corner of the chip.

The **ADC\_ref** pin must be bonded and connected to an off-chip 10 nF capacitor to ground, which should be placed within 1 cm of the lower edge the chip. This capacitor should have an X5R, X7R, C0G, or NP0 dielectric and should be rated for at least 16V. If multiple RHD2164 chips are used, each chip must have its own 10 nF capacitor. The **ADC\_ref** pins of different chips should not be connected.

The **VESD** pad must be bonded and connected either to ground (recommended) or to VDD. See the “Amplifier Input Protection” section of the RHD2000 series datasheet for more information on this pin.

It is not necessary to bond the **auxin1**, **auxin2**, or **auxin3** pins if auxiliary analog signals will not be connected to the chip.

It is not necessary to bond the **auxout** pin of the auxiliary digital output will not be used.

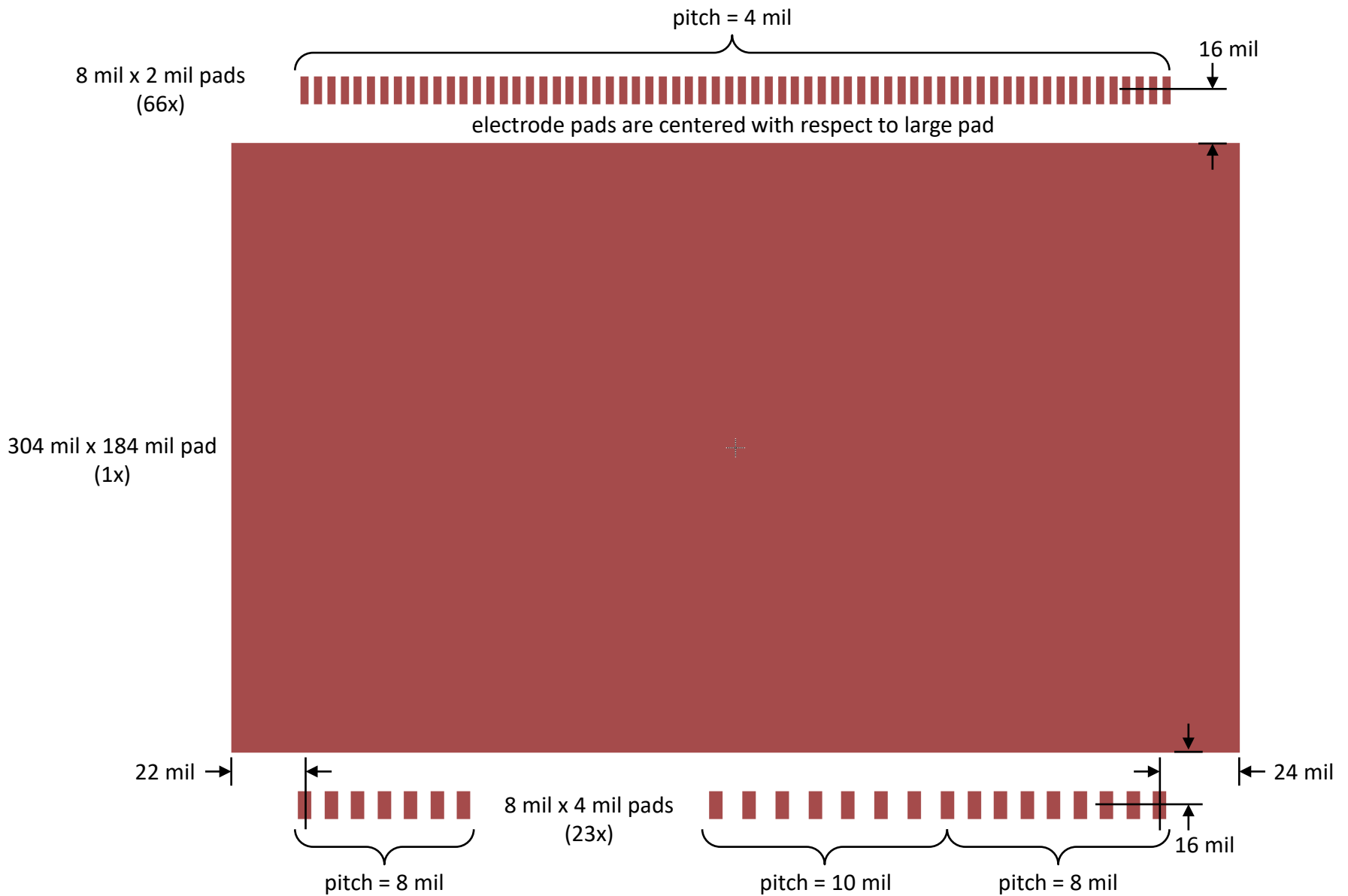
In most applications, the **elec\_test** pad should remain unbonded. This pad is typically used only to provide DC voltages for the purposes of electrode activation or electroplating. See the “Electrode Activation” section of the RHD2000 series datasheet for more details.

The **LVDS\_en** pad of the RHD2164 chip has an internal pull-up resistor that enables LVDS signaling on the SPI bus if this pad is left unbonded. If non-LVDS (standard CMOS) SPI signaling is desired then this pad must be bonded and connected to ground.

If LVDS SPI signaling will be used, than all eight SPI pads ( **$\overline{\text{CS}}$** –,  **$\overline{\text{CS}}$** + , **SCLK**–, **SCLK**+ , **MOSI**–, **MOSI**+ , **MISO**–, **MISO**+ ) must be bonded. If non-LVDS (standard CMOS) SPI signaling will be used, the negative SPI pins ( **$\overline{\text{CS}}$** –, **SCLK**–, **MOSI**–, **MISO**– ) can remain unbonded.

# Suggested PCB Footprint for Chip-on-Board Assembly

dimensions in mils (1 mil = 0.001 inch = 25.4 microns)



Immersion gold finish (ENIG) or similar planar, bondable finish should be used on PCB.